In The Specification:

Please amend paragraph [0021] as follows:

[0021] The microprocessor interface (302) of the control chip (30) receives a first Address strobe (ADS) signal, a request signal (HREQ[4:0]), and an address bus signal (HA[31:3]) from the CPU (32). The HREQ[4:0] includes two phases, Phase I and Phase II, which are respectively called "selection phase" and "length phase". The selection phase is used to determine the transmission type of the HREQ[4:0] signal while the length phase is used to indicate the length of memory being accessed. The address bus signal (HA[31:3] signal) contains two phases Phase I and Phase II, which are respectively called "address phase" and "byte enable phase". The address phase specifies a memory address, while the byte enable phase indicates the data type used for memory accessing, for example, a byte, a word, double word or quad word. The decoder (304) in the microprocessor interface (302) performs the decoding operations onto the first address strobe (ADS) signal, the request signal (HREQ[4:0]), and the address bus signal (HA[31:3]), while the decoding results are subsequently fed into the AND gate (312) through the signal line (312A). The AND gate (312) outputs a high logic state via the second ADS signal referring to the HCLK if the decoding results indicate the request selection phase is either a memory read or memory write signal, and the address phase is also addressed to an effective memory range. In the preferred embodiment, the decoder (304)~~AND gate (312)~~ outputs a logic high state via the EN signal line by referring to the HCLK if there is no Zlen signal suggested. That is, the specific condition that the memory length indicated by the length phase of the

HREQ[4:0] signal is "quad word", and simultaneously all bytes of the byte enable phase in the HA[31:3] signal are disabled (e.g., all bytes are logic low) is detected in Phase II of HREQ[4:0] and HA[31:3]. The signal conversion circuit (306) coupled to the microprocessor interface (302) is used to convert the second ADS signal into a third ADS signal, wherein the second and third ADS signals refer to the HCLK and DCLK, respectively. Moreover, an arbitration circuit (310) mounted in the memory controller (308) receives the third ADS signal and the enable signal EN. When both the third ADS signal and the enable signal EN are enabled (i.e., both in logic high states), the arbitration circuit (310) outputs a memory control signal, which is then directed to the memory to actuate the required memory access operations. Notably, the arbitration circuit (310) can be established by using an AND gate or other logic circuits, while the AND gate (312) can also be mounted inside the decoder, or established by means of another logic circuit. It will be apparent to one of ordinary skill in the art that modifications within the spirit of the embodiment should be included in the appended claims.